CPS-JKII

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
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SYMBOL

BUFFER B
ELEMENT IDENT
A

TERM. MOD.	FUNCT.	TERM.	LOC
BACRO	I	018	3A2
BSHPU	I	019	2A9
C.BR1	I	013	3A1
C.STC1	I	012	2AS
OV.FILL1	I	11S	2A8
FILLO	I	016	2A8
I16BC1	I	105	3A1
MRSTA1	I	01A	2AS
PPEHO	I	002	2A0
PPELO	I	102	2A0
SDØTO	I	118	3A0
ST.CLKO	I	101	2A6
STUFFO	I	107	2A0
SWB1	I	112	3A5
TG.SEQ1	I	104	2A2
UNLØADO	I	001	2A0
BCLK	Ø	116	2H7
BLK.CBR1	Ø	007	3HS
BØFLO	Ø	017	3H4
BRO	Ø	015	3H6
BUSYO	Ø	100	2H3
CLKA1	Ø	109	2H6
CLKITRO	Ø	003	2H3
LDPCKDO	Ø	010	2H1
ØFLCLK:	Ø	103	2H2
ØNLCLKO	Ø	113	3H3
ØNLCMPO	Ø	009	3H1
PE1	Ø	111	2H0
SOINO	Ø	117	3H0
SHIFT1	Ø	004	2H4
STFILLO	Ø	011	2H9
1ACTO	Ø	114	3H4
+5	P	000,119	3H6
GRD	G	200,319	3H7

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT DRAIN: 425mA

NOTES:

1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

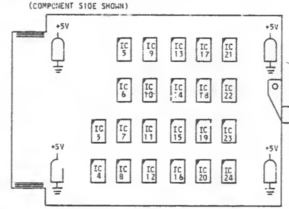
IC CODE	BAT. TERM.	GRD TERM.
41A0	16	8
41AE	16	7,8
41BP	16	8
41BR	16	7,8
41CA	16	8
41CB	16	8
41CC	16	8
41CJ	16	8
41EH	16	7,8
41U	16	8
41W	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.

6. INTEGRATED CIRCUIT LOCATION GUIDE:
(COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

DWG ISSUE	EE OR CD ISSUED	DATE ISSUE		APPD
	—	10-9-74	LRE LRE	RWF MTS RFG
2B1	—	4-8-76	P/S LRE	JLT LEG RFG
3A1		2-11-77	AS LRE	WJZ LEG RFG
4A	—	4-6-77	AS LRE	WJZ LEG RFG

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK11
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE).	
ACCEPTABLE SERIES	3

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

ISSUE 4A

1N98

JK11 CIRCUIT PACK

BUFFER B
CIRCUIT

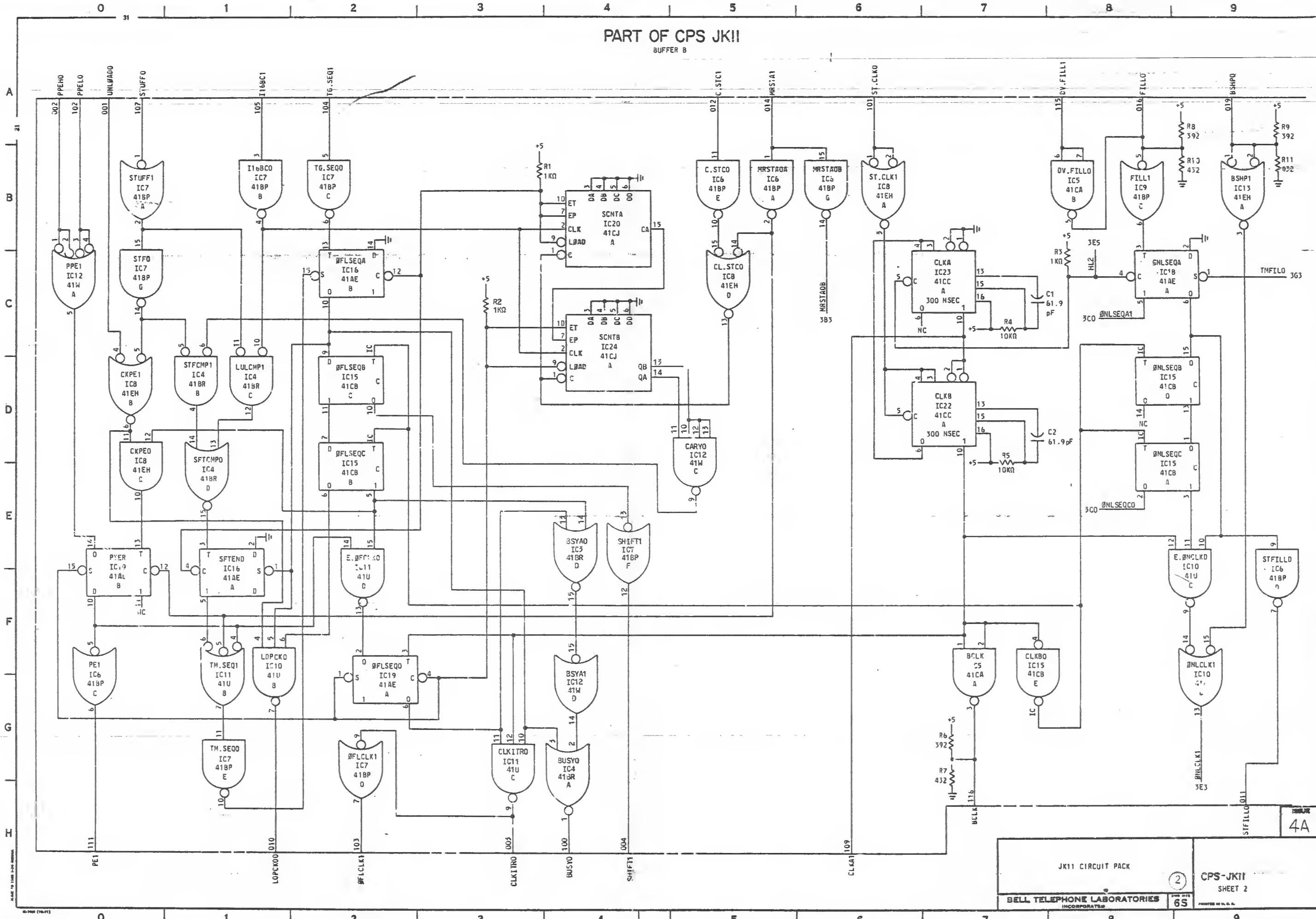
AT&TCO
STANDARD

(2) CPS-JKII
4 SHEETS

BELL TELEPHONE LABORATORIES
INCORPORATED

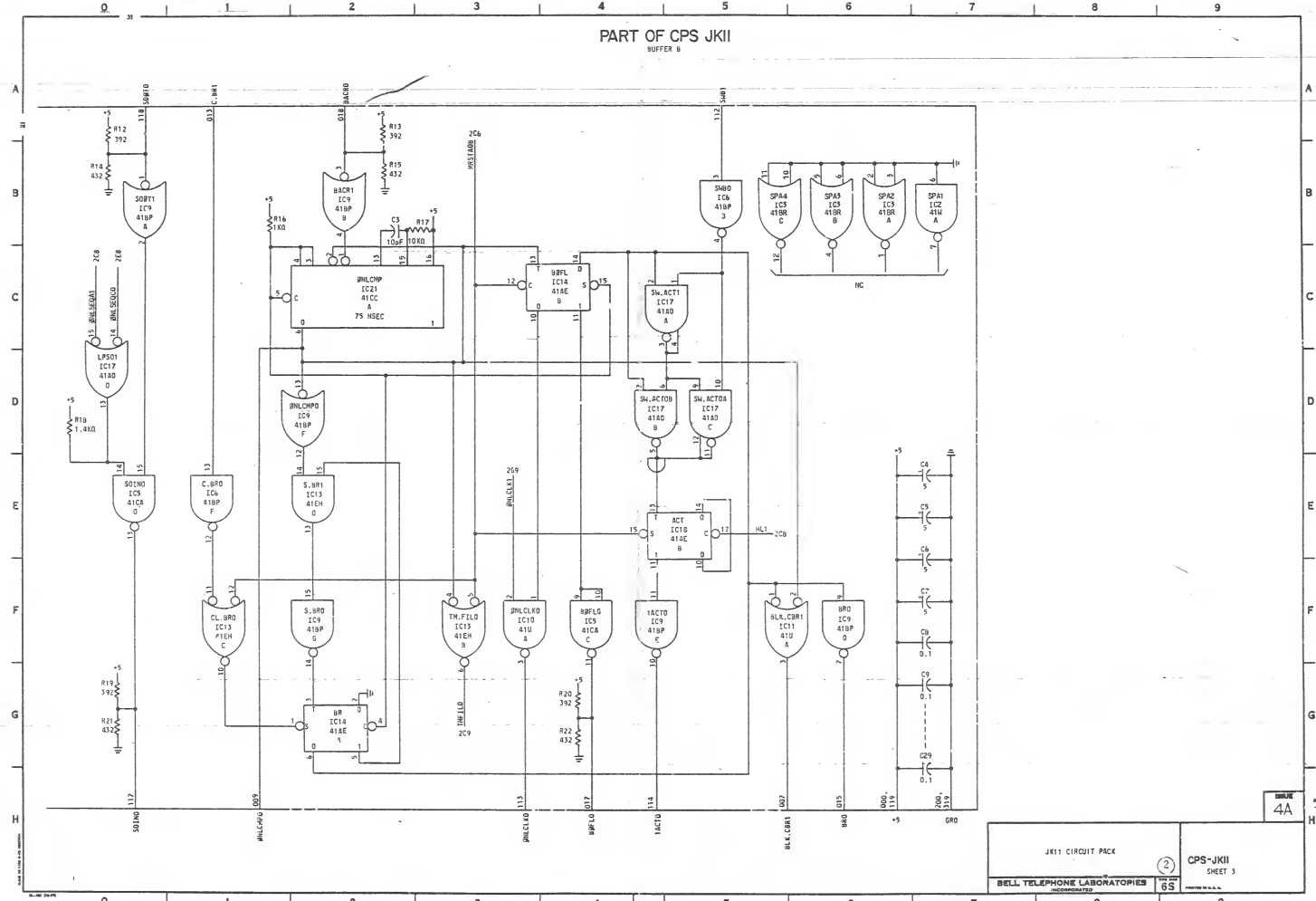
6S

CPS-JKII



PART OF CPS JK11
BUFFER B
PPEHO
PPELO
UNLØADO
STUFFO
I16BC1
TG.SEQ1
C.STC1
MRSTA1
ST.CLKO
DV.FILL1
FILLO
BSHPQ
STUFF1 IC7 41BP A
I16BCO IC7 41BP B
TG.SEQO IC7 41BP C
SCNTA IC20 41CJ A
SCNTB IC24 41CJ A
C.STCO IC6 41BP E
MRSTAOA IC6 41BP A
MRSTAOB IC6 41BP G
ST.CLK1 IC8 41EH A
DV.FILLO IC5 41CA B
FILL1 IC9 41BP C
BSHP1 IC13 41EH A
PPE1 IC12 41W A
STFO IC7 41BP G
ØFLSEQA IC16 41AE B
CL.STCO IC8 41EH D
CLKA IC23 41CC A 300 NSEC
CLKB IC22 41CC A 300 NSEC
ØNLSEQA IC18 41AE A
CKPE1 IC8 41EH B
STFCMP1 IC4 41BR B
LULCMP1 IC4 41BR C
ØFLSEQB IC15 41CB C
ØNLSEQB IC15 41CB D
ØNLSEQC IC15 41CB A
CKPEO IC8 41EH C
SFTCMPO IC4 41BR D
ØFLSEQC IC15 41CB B
CARYO IC12 41W C
PYER IC19 41AE B
SFTEND IC16 41AE A
BSYAO IC3 41BR D
SHIFT1 IC7 41BP F
E.ØNCLKO IC10 41U C
STFILLO IC6 41BP D
PE1 IC6 41BP C
TM.SEQ1 IC11 41U B
LDPCKO IC10 41U B
ØFLSEQO IC19 41AE A
BSYA1 IC12 41W D
BCLK C5 41CA A
CLKBO IC15 41CB E
ØNLCLK1 IC10
TM.SEQO IC7 41BP E
ØFLCLK1 IC7 41BP D
CLKITRO IC11 41U C
BUSYO IC4 41BR A
C1 61.9 pF
C2 61.9 pF
R1 1KΩ
R2 1KΩ
R3 1KΩ
R4 10KΩ
R5 10KΩ
R6 392
R7 432
R8 392
R9 392
R10 432
R11 432
TMFILO 3G3
MRSTAOB 3B3
3CO ØNLSEQA1
3CO ØNLSEQCO
ØNLCLK1 3E3
PE1
LDPCKOO
ØFLCLK1
CLKITRO
BUSYO
SHIFT1
CLKA1
BCLK
STFILLO
JK11 CIRCUIT PACK
CPS-JK11
SHEET 2
ISSUE 4A
BELL TELEPHONE LABORATORIES INCORPORATED
6S

CPS-JK11


PART OF CPS JKII
BUFFER B
SDBT0
C.BR1
BACR0
SWB1
R12 392
R14 432
SDBT1 IC9 41BP A
R13 392
R15 432
BACR1 IC9 41BP B
R16 1KΩ
C3 10pF
R17 10KΩ
2C6
HOLDADR
SWB0 IC6 41BP 3
SPA4 IC3 41BR C
SPA3 IC9 41BR B
SPA2 IC3 41BR A
SPA1 IC2 41W A
NC
2C8
2E8
BNLSEQA1
BNLSEQA0
BNLCMP IC21 41CC A 75 NSEC
BBFL IC14 41AE B
SW.ACT1 IC17 41AD A
LPS01 IC17 41AD D
R18 1.4KΩ
BNLCMPD IC9 41BP F
SW.ACT0B IC17 41AD B
SW.ACT0A IC17 41AD C
SDIN0 IC5 41CA D
C.BR0 IC6 41BP F
S.BR1 IC13 41EH B
2G9
BNLCLK1
ACT IC16 41AE B
HL1
2C8
C4 .1
C5 .1
C6 .1
C7 .1
C8 0.1
C9 0.1
C29 0.1
CL.BR0 IC13 41EH C
S.BR0 IC9 41BP D
TM.FILO IC13 41EH B
BNLCLK0 IC10 41U A
BBFLG IC5 41CA C
1ACT0 IC9 41BP E
BLK.CBR1 IC11 41U A
BR0 IC9 41BP D
BR IC14 41AE A
R19 392
R21 432
R20 392
R22 432
1MFIL0
2C9
SDIN0
BNLCAFU
BNLCLK0
BBFL0
1ACT0
BLK.CBR1
BR0
+5
GR0
4A
JK11 CIRCUIT PACK
BELL TELEPHONE LABORATORIES
INCORPORATED
2
6S
CPS-JKII
SHEET 3

CPS-JKII

PART OF CPS JKII

BUFFER B

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC3 41BR DESIG	SH LOC	IC4 41BR DESIG	SH LOC	IC5 41CA DESIG	SH LOC	IC6 41BP DESIG	SH LOC	IC7 41BP DESIG	SH LOC	IC8 41EH DESIG	SH LOC	IC9 41BP DESIG	SH LOC	IC10 41U DESIG	SH LOC	IC11 41U DESIG	SH LOC	IC12 41W DESIG	SH LOC	IC13 41EH DESIG	SH LOC	IC14 41AE DESIG	SH LOC
A	SF2	3B6	BUSY0	2B4	BCLK	2F7	MRSTA0A	2B9	STUFF1	2B0	ST.CLK1	2B6	SQ@T1	9B0	@NLCLK0	3F3	BLK.CSR1	3F5	PPE1	2C0	BSHP1	2B9	BR	3G2
B	SF3	3B6	STFCMP1	2D1	DV.FILL0	2B8	SWB0	3B9	I16BC0	2B1	CKPE1	2D0	A=B1	3B2	LDPCK0	2F1	TM.SEQ1	2F1	SP1	3B7	TM.FIL0	3F3	B@FL	4C4
C	SF4	3B5	LULCMP1	2D1	B@FL0	3F4	PE1	2F0	TG.SEQ0	2B2	CKPE0	2D0	FILL1	2B8	E.@NCLK0	2E9	CLKITR0	2G3	CARY0	2D5	CL.BR0	3F1		
D	SSYA0	2E4	SFTCMP0	2D1	SOTN0	9E0	@FLCLK1	2B2	TM.SEQ0	2D1	CL.STC0	2C9	BR0	3F6	@NLCLK1	2F9	E.@FCLK0	2E2	SSYA1	2F4	S.BR1	3E2		
E							C.STC0	2B5	SHIFT1	2E4			IACT0	3F4										
F							C.BR0	3E1	STF0	2C0			@NLCMP0	3G2										
G							MRSTA0B	2B6					S.BR0	3F2										

LOC CODE ELEM ID	IC15 41CB DESIG	SH LOC	IC16 41AE DESIG	SH LOC	IC17 41A0 DESIG	SH LOC	IC18 41AE DESIG	SH LOC	IC19 41AE DESIG	SH LOC	IC20 41CJ DESIG	SH LOC	IC21 41CC DESIG	SH LOC	IC22 41CC DESIG	SH LOC	IC23 41CC DESIG	SH LOC	IC24 41CJ DESIG	SH LOC
A	@NLSEQC	2D9	SFTEN0	2E1	SW.ACT1	3C5	@NLSEQA	2C9	@FLSEQD	2F2	SCNTA	2B4	@NLCMP	3C2	CLKB	2D7	CLKA	2C7	SCNTB	2C4
B	@FLSEQC	2D2	@FLSEQA	2C2	SW.ACT0B	3D4	ACT	3E5	PTER	2E0										
C	@FLSEQB	2D2			SW.ACT0A	3D5														
D	@NLSEQB	2D9			LPS01	3D0														
E	CLK80	2F7																		
F																				
G																				

CAPACITOR

	DESIG	CODE
[2]	C1,C2	KS-16958 L27, 61.5pF
	C3	KS-16958 L27, 10pF
[4]	C4-C7	6018, S
[22]	C8-C29	KS-19774 L5, 0.1

RESISTOR

	DESIG	CODE
[3]	R1-R3	KS-20616 L14, 1KΩ
[2]	R4,R5	.10KΩ
	R6	.392
	R7	.432
[2]	R8,R9	.392
[2]	R10,R11	.432
[2]	R12,R13	.392
[2]	R14,R15	.432
	R16	.1KΩ
	R17	.10KΩ
	R18	.1.4KΩ
[2]	R19,R20	.392
[2]	R21,R22	KS-20616 L14, 432

CIRCUIT DESCRIPTION

CIRCUIT PACK JK11 HANDLES BUFFER SEQUENCING. MONOPULSERS CLK4 AND CLK8 GENERATE A 600 ns (NOMINAL) SQUARE WAVE CLOCK PULSE TRAIN WHICH IS DISTRIBUTED TO BOTH THE ON-LINE AND OFF-LINE SEQUENCER CHAINS (@NLSEQ, @FLSEQ), AND ALSO DRIVES OFF THE BOARD ON BUFFER SERIAL BUS LEAD BCLK. THE CLOCK IS STOPPED WHILE ST.CLK0 IS ACTIVE. NEGATION OF ST.CLK0 RESTARTS THE CLOCK.

MOVEMENT OF DATA INTO OR OUT OF THE ON-LINE BUFFER IS CONTROLLED BY THE PERIPHERAL UNIT ENGAGING IT. THE ON-LINE CLOCK @NLCLK0 IS DERIVED FROM THE SHIFT PULSES APPEARING ON SERIAL BUFFER BUS LEAD BSHP0. @NLCLK0 IS INHIBITED IF AN OVERFLOW CONDITION EXISTS.

THE ON-LINE SEQUENCER OPERATES WHEN EITHER THE PERIPHERAL OR CC REQUESTS AN ON-LINE BUFFER FILL OPERATION BY CLEARING @NLSEQA VIA LEAD FILL0 OR DV.FILL RESPECTIVELY. @NLSEQB AND @NLSEQC ARE CONSECUTIVELY SET, THE LATTER ENABLING @NLCLK0 TO BE DRIVEN BY THE BUFFER CLOCK VIA GATE E.@NCLK0. EITHER @NLSEQA BEING CLEAR OR @NLSEQC BEING SET ENABLES A RECIRCULATION PATH FROM BUFFER OUTPUT SOBT0 BACK INTO INPUT SOTN0 DURING THE FILL OPERATION. AN ON-LINE SEQUENCE IS TERMINATED BY A PULSE ON TMFIL0 WHICH IS GENERATED BY ON-LINE OPERATION COMPLETE MONOPULSER @NLCMP.

@NLCMP IS TRIGGERED ON THE TRAILING EDGE OF THE ON-LINE BUFFER 1024-BIT CARRY BACR0. THE TRAILING EDGE OF THE @NLCMP PULSE RAISES THE BR FLAG (BR F/F CLEARED) AND CLOCKS THE B@FL F/F. IF BR IS RAISED WHEN B@FL IS CLOCKED, AN OVERFLOW CONDITION IS INDICATED, B@FL IS SET, AND B@FL0 IS ASSERTED.

THE ON-LINE/OFF-LINE STATUS OF THE TWO 1024-BIT BUFFERS ON JK13 IS GOVERNED BY THE STATE OF THE ACT F/F. THE TOGGLE INPUT TO ACT IS FORMED BY THE LOGICAL EXCLUSIVE BR OF THE STATES OF SW81 AND THE BR F/F OUTPUT. IF EITHER LEAD GOES HIGH, ACT TOGGLES AND THE BUFFERS SWITCH ON-LINE AND OFF-LINE STATUS.

CIRCUIT DESCRIPTION (CONT):

A PULSE ON IC SEQ0 ACTIVATES THE OFF-LINE SEQUENCER CHAIN BY CLOCKING @FLSEQA. @FLSEQB AND @FLSEQC PROVIDE DELAY IN THE SEQUENCE TO ALLOW SETTLING TIME FOR THE PARITY TREES ON JK12. PARALLEL PARITY ERRORS INDICATED BY THE STATES OF PPEL0 OR PPEH0 CAUSE PTER TO BE SET BY @FLSEQC DURING LOAD OPERATIONS. LDPCK0 DELAYS THE STATUS REPLY CHAIN ON JK10 TO INSURE THAT PARITY ERROR STATUS IS REPORTED TO THE CC BY THE SST IMMEDIATELY FOLLOWING THE LOAD OPERATION. A REGISTERED PARITY ERROR TERMINATES THE SEQUENCE BY SETTING @FLSEQA. OTHERWISE, @FLSEQD IS CLOCKED AND ENABLES OFF-LINE AND ITM CLOCKS @FLCLK1 AND CLKITR0 WHICH ARE THEN DRIVEN BY THE 600 ns PULSE TRAIN. OFF-LINE SEQUENCES GOVERNED BY THE LOAD OR UNLOAD STATES CAUSE THE SFTEN0 F/F TO BE CLOCKED ON THE TRAILING EDGE OF THE OFF-LINE BUFFER 16-BIT CARRY PULSE ON I16BC1 TO TERMINATE THE SEQUENCE. STUFF OPERATIONS ARE TERMINATED BY THE TRAILING EDGE OF THE STUFF COUNTER CARRY PULSE. THE STUFF COUNTER DIVIDES BY 16 IN SCNTA AND BY 4 IN SCNTB IN ORDER TO COUNT THE APPEARANCE OF 64 PULSES ON I16BC1.

AN ACTIVE LEVEL ON LEAD MRSTA1 INITIALIZES BOTH ON-LINE AND OFF-LINE SEQUENCERS AS WELL AS THE STUFF COUNTER AND THE BR, ACT, B@FL, AND PTER F/Fs.

ISSUE 4A

JK11 CIRCUIT PACK

BELL TELEPHONE LABORATORIES UNCLASSIFIED

CPS-JKII SHEET 4

CPS-JKII